High Efficiency GaAs MBE Power FETs for Ka-Band

J. Geddes, V. Sokolov, T. Contolatis and J. Abrokwah
Honeywell Physical Sciences Center
and
W. Larson
Honeywell Corporate Solid State Laboratory

ABSTRACT

Submicron gate length, 300 micron gate width GaAs FETs were fabricated on MBE material using direct write e-beam lithography. Evaluation of the devices in a Ka-band test fixture with fin line transitions resulted in an amplifier output power of 110 mw with 11 percent power added efficiency at 30 GHz. At 2.9 dB gain the power per unit gate width is .46 W/mm referenced to the device. This is the highest power output per unit gate width reported to date for a GaAs FET at Ka-band.

INTRODUCTION

Steady progress in GaAs power FET development has brought device operation to Ka-band frequencies. However, recent results [1,2] at Ka-band have shown reduced power added efficiency and power per unit gate width compared to results at lower frequencies. Device measurements at frequencies up to 16 GHz have indicated that 1 watt per millimeter gate width can be obtained with very little frequency dependence [3]. Power added efficiencies of 40 percent at 15 GHz [4] and 26.6 percent at 21 GHz [5] have been achieved. The frequency limits on power per unit gate width and efficiency form a critical question in GaAs power FET development. The answer to this question will play an important role in directing the development of future satellite communication systems and phased array radars.

Most of the best power FETs reported to date are fabricated on VPE material, but recently good results at Ka-band [5] have been reported using MBE material. This paper reports on power FETs fabricated on MBE material with the highest saturated output power per unit gate width reported to date (.46 W/mm) at Ka-band. At the 1 dB gain compression point, the power output was 100 mW.

DEVICE FABRICATION

The MBE material was grown on a PHI model 425 MBE system. A .5 micron thick buffer layer was grown on 3 inch LEC substrate material followed by a .3 micron thick channel layer doped to a carrier concentration of $3.6 \times 10^{17} cm^{-3}$. The layers were grown at a 600°C substrate temperature with a 1 micron per hour growth rate. The V/III(As/Ga) flux ratio was 15 as determined by an ion gauge; As_4 was used for the arsenic source. A carrier concentration profile of the material as determined by C-V measurements is shown in Figure 1. Additional details of the material growth will be reported in a future publication [6].

Devices were fabricated using direct write e-beam lithography for all but the pad metal level. Exposures were done on a Cambridge EBMF-6 system. A set of ion milled pits on the wafer were used for alignment marks. Device isolation was achieved using a mesa etch with polystyrene as the negative e-beam resist. Ohmic contacts for source and drain were formed using an e-beam evaporated Ge/Au/Ni contact sandwich defined by liftoff using a proprietary 2-layer resist process which allowed rapid exposure of the ohmic level without substrate charging effects. The gate level was defined using PMMA resist for liftoff. Prior to gate metallization, the gate area was recess etched to bring the saturated drain current down to 100-130 ma for the completed devices. A 500Å Ti/3500Å Au pad metal level was applied using optical lithography with 1450J photoresist and a chlorobenzene soak to improve the resist profile. Prior to dicing and mounting, the wafer was thinned to .1mm to ensure low thermal resistance and backside metal was applied. A photomicrograph of the completed 300 micron PI gate device and typical DC IV are shown in Figures 2 and 3. The .5 micron gate is placed in a 3.5 micron wide source-drain gap with a 1 micron gate-source spacing. The DC IV indicates a transconductance of 133 mmho/mm and a low saturation voltage of about 1.2 volts. The saturation current of the device is 333 ma/mm.

RF TEST FIXTURES AND RESULTS

Two test fixtures are used to evaluate the RF performance of the 300 μm gate width FETs at 15 and 30 GHz. At 15 GHz a typical microstrip hybrid circuit incorporating .25 mm thick alumina substrates and a pair of microstrip to SMA coax transitions are used to interface the FET chip with the test equipment. Simple quarter wave microstrip transformers and bond wire inductance are used to impedance match the device.

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At 30 GHz an in-line waveguide-compatable test fixture incorporating antipodal fin-line transitions etched on RT/duroid are used to transition from Ka-band waveguide to microstrip [7,8]. Impedance matching circuits are etched on 0.25 mm thick fused quartz substrates which interface the 50 ohm microstrip transmission line of the RT/duroid with the FET chip. The matching circuits make use of single section quarter wavelength coupled lines (f =35 GHz) [9] to reduce the real part of the impedance from 50 ohms to 8 ohms on both input and output. An advantage of the coupled line approach is that the transverse dimension of the resulting microstrip pattern is much less than a quarter wavelength at the operating frequency (strip width is 0.33 mm and gap is 0.05 mm). In comparison the corresponding single line quarter wavelength microstrip transformer has a strip width approaching its length. Such a configuration can support unwanted transverse resonances. The strip width of the coupled line turns out to be comparable to the transverse dimension of the FET chip, a fortunate condition which minimizes the parasitics associated with the interface connection. Still another advantage of the coupled line is that it provides a DC block for biasing purposes.

A total of four bond wires connect the gate and drain pads of the FET to the input and output matching circuits respectively. Their lengths are adjusted so that the bond wire inductance resonates the device capacitance. A fine gold ribbon mesh connects the source pads to ground to minimize source lead inductance. At center band and under small signal conditions the amplifier's input return loss is 10-15 dB and the output return loss at least 8 dB. Based on individual insertion loss measurements of the various transmission line components, the total fixture loss is 1 to 1.3 dB at 30 GHz. Figure 4 shows the Ka-band amplifier with the cover removed.

At 15 GHz the output power of the FETs is typically 150 mW with a gain of 4.5 - 5.0 dB. A gain of 9-10 dB is obtained when the devices are tuned for maximum small signal gain at 15 GHz. At 31 GHz a small signal gain of 5 to 6 dB gain is obtained for the Ka-band amplifier with a 1 dB bandwidth of 1.5 GHz.

Figure 5 shows the gain compression curve for the Ka-band amplifier with the best power performance when the bias is adjusted for maximum output power. Other than adjustment of the bond wires, no additional tuning was done, and the same 8 ohm coupled line transformers were used. The small signal gain is 4.7 dB and the output 1 dB gain compression point is 100 mW. At an input power of 50 mW (17 dBm) the corresponding output power is 110 mW (20.4 dBm). At this drive level the power added efficiency is 11%. Note that referenced to the device (assuming a 1 dB fixture loss) the corresponding performance is 120 mW output power with a gain of 4.4 dB and a power added efficiency of 15%. Finally the amplifier was driven to a maximum input power of 19 dBm with a corresponding output power of 20.9 dBm (123 mW). At the device level, this corresponds to an output power of 138 mW (.46 W/mm gate width at 30 GHz) with an associated gain of 2.9 dB. It is interesting to note that these MBE FETs have less than 1 dB degradation in the power per unit gate width performance over the octave bandwidth spanning 15-30 GHz.

CONCLUSION

Submicron gate length FETs fabricated on MBE material have achieved the highest saturated power output per unit gate width (.46 W/mm) reported to date at Ka-band. The maximum power added efficiency was 11 percent with 110 mW output including fixture losses of 1 dB. Translated to the device level the power added efficiency is 15 percent. These results indicate the potential of MBE growth for developing high frequency power FETs.

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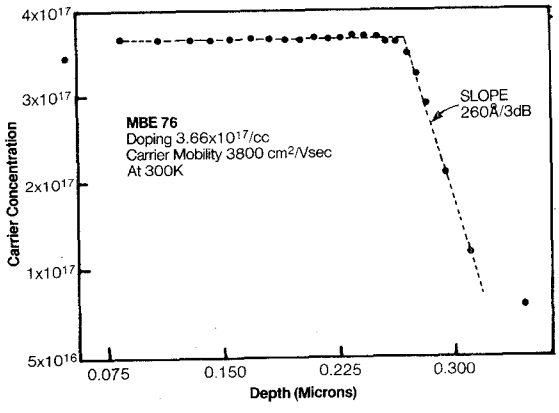

Figure 1. MBE Wafer Carrier Concentration Profile

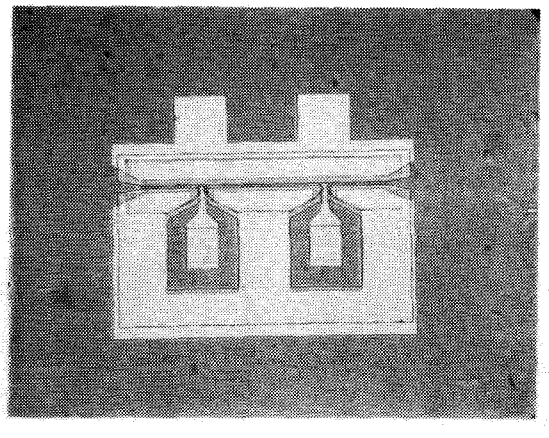

Figure 2. 300 Micron Gate Width PI Gate FET

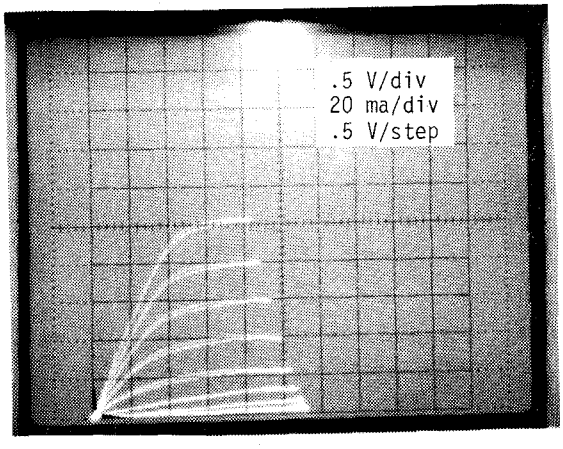

Figure 3. Power FET DC IV

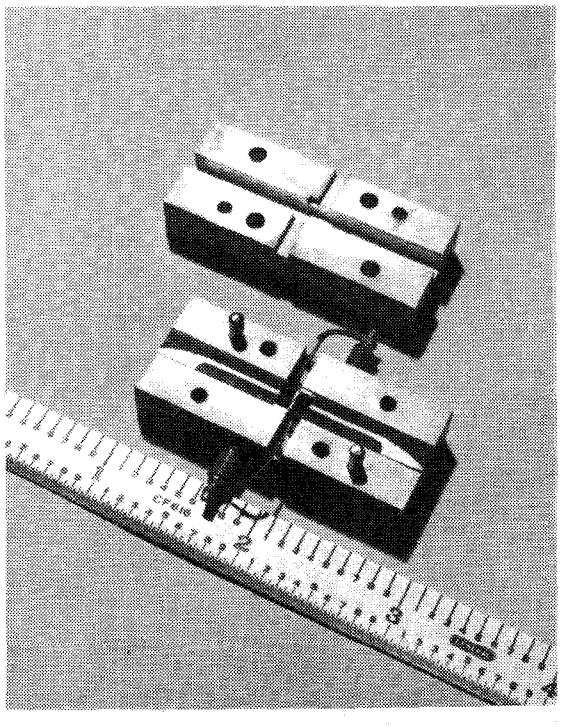

Figure 4. Ka-Band Test Fixture for Amplifier Measurements

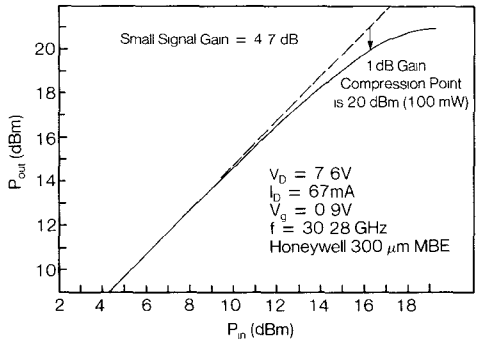

Figure 5. Gain Compression Curve For Ka-Band FET